# InP-based monolithically integrated RTD/HBT MOBILE for logic circuits

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**Abstract:**

The use of negative-differential resistance devices, i.e. Resonant Tunnelling Diodes (RTD) has recently enabled a substantial improvement of low-power memories and high-speed logic gates. These achievements are based on a novel, yet reliable and compact logic module composed of two series connected RTD monolithically integrated with parallel HFET input branches building the monostable-bistable transition logic element (MOBILE [1]).

For low-voltage, high-speed logic application the use of enhancement type HFET is essential in order to provide level compatibility within low complexity circuits [2]. On InP-substrate the realisation of mature enhancement type HFET is a critical issue [2] because of the low Schottky barriers available. On the contrary, the HBT is a principle enhancement type device relaying on the large barrier of the pn-junction. Hence, a couple of digital circuit concepts are under discussion for RTD in combination with HBT on InP-substrate [3]. However, all concepts demand a very precise control of current-voltage data of two independent devices.

In this contribution we report on the application of HBT as input terminals for the MOBILE instead of HFET. In our approach we have chosen a series connection of HBT and RTD (RTBT) as input terminal for the MOBILE (cf. Fig. 1a, shaded area). At high input levels the RTBT characteristics is dominated by the RTD behaviour. As a consequence:

(1) the HBT function is restricted to a switch,

(2) the precise current control for gate operation is due to the RTD area, only.

The logic function of the of the gate (cf. Fig.1) is simplified to the comparison of the sum RTD current (or area) in the opened RTBT1 to RTBT3 on the one hand to the current of the driver RTD1 on the other hand. It is obvious that only the ratio of RTD area is significant for the operation, so technological fluctuations are ruled out. In addition, the peak-to-valley current ratio of the parallel combination of the driver RTD and the input stages device is retained which results in a higher driving capability of the circuit compared to conventional 3-terminal input branches. Moreover, only one polarity is necessary for the supply voltage.

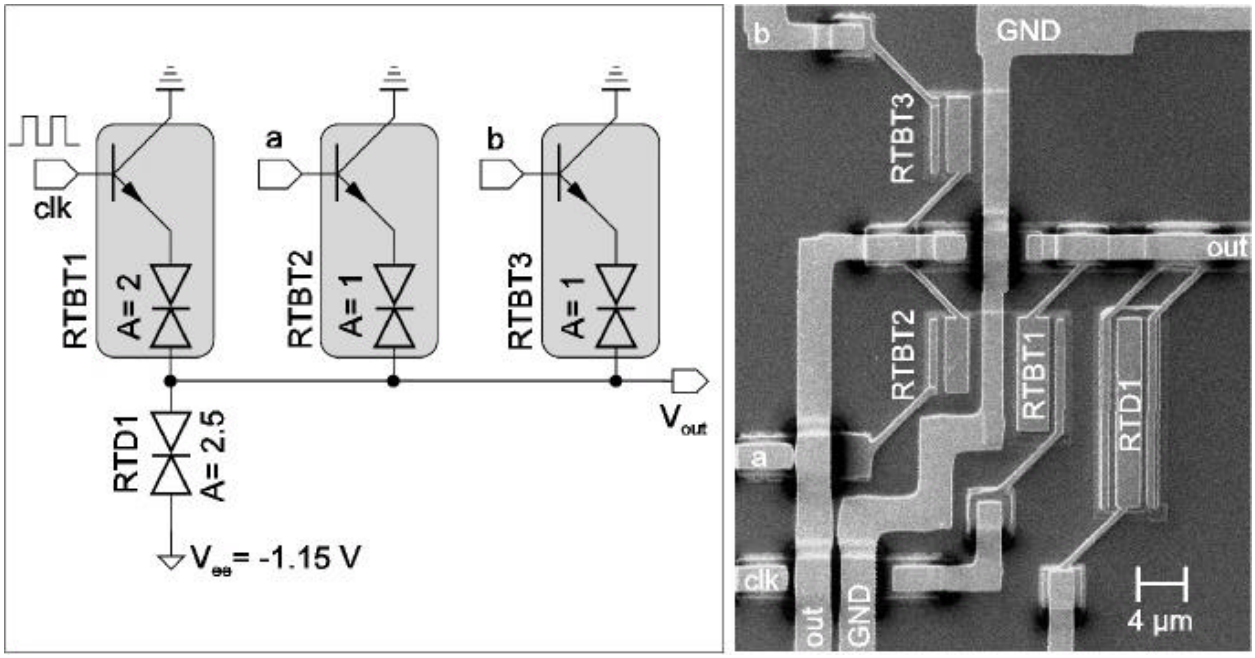
The fabrication of the demonstrator circuits started with the growth of the RTD/HBT layer stack. The InP/InGaAs:C HBT is grown by MOVPE with non gaseous sources followed by an InAlAs/InGaAs RTD grown by MBE. This enables a flexible use of single RTD, HBT or coupled RTD/HBT (RTBT) devices. Device fabrication is done using direct write ebeam lithography and all wet chemical etching. The RTBT reaches small signal transit frequencies up to $f_T$= 40 GHz. The measured device characteristics are implemented in commercial circuit simulation software (PSPICE). Extended device models are developed to the simulate the IV-characteristics of a RTD by the use of an analytical approach and the modelled RTBT characteristics fits precisely to the experimental data.

Novel Boolean logic Gates are designed, realised and tested based on the RTBT device and the MOBILE concept (Fig. 1). In Figure 2 the timing diagram obtained by H-SPICE simulations are compared to experimental data. In Fig. 2 the functionality of the NOR gate is proven at low frequencies and other gate functions are available depending on the design of the RTD area (cf. Fig. 1) SPICE simulations based on measured single device characteristics indicate, that our approach allows multi Gb/s operation with robust logic levels.

[1] K.J.Chen, T.Akeyoshi, K.Maezawa; "Monolithic integration of resonant tunneling diodes and FET's for monostable-bistable transition logic elements (MOBILE's)", IEEE Electron Dev. Lett., vol.16, no.2, 1995, p.70.

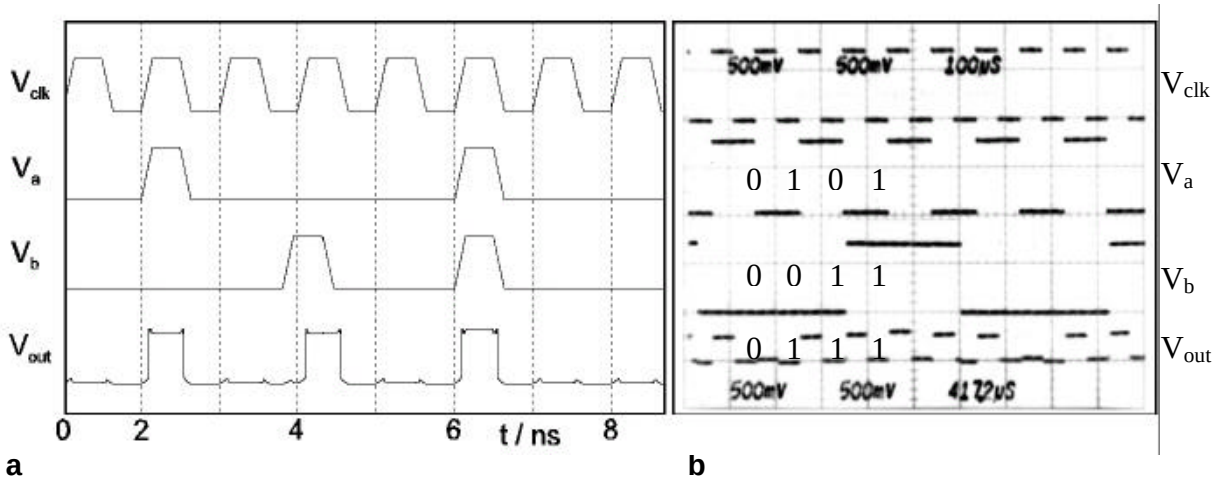
[2] W.Prost, U.Auer, C.Pacha, A.Brennemann, K.Goser, F.-J.Tegude, "Novel MOBILE Gates with Low-Power, Relaxed Parameter Sensitivity, and Increased Driving Capability ", in Proc. 11th Int. Conf. on InP and Rel. Mat.', Davos, Switzerland, IEEE Catalog No. 99CH36362, pp.411, 1999.

[3] P.Mazumder, S.Kulkarni, M.Bhattacharya, J.P.Sun, G.I.Haddad, "Digital Circuit Applications of Resonant Tunnelling Devices", Proceedings of the IEEE, Vol.86, No.4, April 1998, pp.664-686.




**a** **b**

Fig. 1: Design (**a**) and SEM micrograph (**b**) of an NOR-Gate in MOBILE configuration consisting of a clock RTBT (RTBT1), two input nodes (RTBT2, 3) and the driver RTD (RTD1). The peak current of the devices is scaled by the ratio of their area *A*. Nominally *A* = 1 corresponds to 30 µm².




**a** **b**

Fig. 2: H-SPICE simulation (a) and measured low frequency (b) timing diagram of a NOR gate (ouptut inversion not shown).